

Introduction to Intel x86-64 Assembly, Architecture, Applications, & Alliteration

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Guess what?

I have repeatedly misled you!

- Simplification is misleading
- Time to learn the *fascinating* truth...
- Time to RTFM!

Read The Fun Manuals

- <http://www.intel.com/products/processor/manuals/>
- Vol.1 is a summary of life, the universe, and everything about x86
- Vol. 2a & 2b explains all the instructions
- Vol. 3a & 3b are all the gory details for all the extra stuff they've added in over the years (MultiMedia eXtensions - MMX, Virtual Machine eXtensions - VMX, virtual memory, 16/64 bit modes, system management mode, etc)
- Reminder, we're using the pre-downloaded May 2012 version as the standardized reference throughout this class so we're all looking at the same information
- We'll only be looking at Vol. 2a & 2b in this class

Interpreting the Instruction Reference Pages

- The correct way to interpret these pages is given in the Intel Manual 2a, section 3.1
- I will give yet another simplification
- Moral of the story is that you have to RTFM to RTFM ;)

Here's what I said:

AND - Logical AND

- Destination operand can be r/mX or register
- Source operand can be r/mX or register or immediate (No source *and* destination as r/mXs at the same time)

and al, bl

00110011b (al - 0x33)

AND 01010101b (bl - 0x55)

result 00010001b (al - 0x11)

and al, 0x42

00110011b (al - 0x33)

AND 01000010b (imm - 0x42)

result 00000010b (al - 0x02)

Here's
what
the
manual
says:

AND—Logical AND

Opcode	Instruction	Op/ En	64-bit Mode	Compat/ Leg Mode	Description
24 <i>ib</i>	AND AL, <i>imm8</i>	RM	Valid	Valid	AL AND <i>imm8</i> .
25 <i>iw</i>	AND AX, <i>imm16</i>	RM	Valid	Valid	AX AND <i>imm16</i> .
25 <i>id</i>	AND EAX, <i>imm32</i>	RM	Valid	Valid	EAX AND <i>imm32</i> .
REX.W + 25 <i>id</i>	AND RAX, <i>imm32</i>	RM	Valid	N.E.	RAX AND <i>imm32</i> sign-extended to 64-bits.
80 /4 <i>ib</i>	AND <i>r/m8</i> , <i>imm8</i>	MR	Valid	Valid	<i>r/m8</i> AND <i>imm8</i> .
REX + 80 /4 <i>ib</i>	AND <i>r/m8*</i> , <i>imm8</i>	MR	Valid	N.E.	<i>r/m8</i> AND <i>imm8</i> .
81 /4 <i>iw</i>	AND <i>r/m16</i> , <i>imm16</i>	MR	Valid	Valid	<i>r/m16</i> AND <i>imm16</i> .
81 /4 <i>id</i>	AND <i>r/m32</i> , <i>imm32</i>	MR	Valid	Valid	<i>r/m32</i> AND <i>imm32</i> .
REX.W + 81 /4 <i>id</i>	AND <i>r/m64</i> , <i>imm32</i>	MR	Valid	N.E.	<i>r/m64</i> AND <i>imm32</i> sign-extended to 64-bits.
83 /4 <i>ib</i>	AND <i>r/m16</i> , <i>imm8</i>	MR	Valid	Valid	<i>r/m16</i> AND <i>imm8</i> (sign-extended).
83 /4 <i>ib</i>	AND <i>r/m32</i> , <i>imm8</i>	MR	Valid	Valid	<i>r/m32</i> AND <i>imm8</i> (sign-extended).
REX.W + 83 /4 <i>ib</i>	AND <i>r/m64</i> , <i>imm8</i>	MR	Valid	N.E.	<i>r/m64</i> AND <i>imm8</i> (sign-extended).
20 / <i>r</i>	AND <i>r/m8</i> , <i>r8</i>	MI	Valid	Valid	<i>r/m8</i> AND <i>r8</i> .
REX + 20 / <i>r</i>	AND <i>r/m8*</i> , <i>r8*</i>	MI	Valid	N.E.	<i>r/m64</i> AND <i>r8</i> (sign-extended).
21 / <i>r</i>	AND <i>r/m16</i> , <i>r16</i>	MI	Valid	Valid	<i>r/m16</i> AND <i>r16</i> .
21 / <i>r</i>	AND <i>r/m32</i> , <i>r32</i>	MI	Valid	Valid	<i>r/m32</i> AND <i>r32</i> .
REX.W + 21 / <i>r</i>	AND <i>r/m64</i> , <i>r64</i>	MI	Valid	N.E.	<i>r/m64</i> AND <i>r32</i> .
22 / <i>r</i>	AND <i>r8</i> , <i>r/m8</i>	I	Valid	Valid	<i>r8</i> AND <i>r/m8</i> .
REX + 22 / <i>r</i>	AND <i>r8*</i> , <i>r/m8*</i>	I	Valid	N.E.	<i>r/m64</i> AND <i>r8</i> (sign-extended).
23 / <i>r</i>	AND <i>r16</i> , <i>r/m16</i>	I	Valid	Valid	<i>r16</i> AND <i>r/m16</i> .
23 / <i>r</i>	AND <i>r32</i> , <i>r/m32</i>	I	Valid	Valid	<i>r32</i> AND <i>r/m32</i> .
REX.W + 23 / <i>r</i>	AND <i>r64</i> , <i>r/m64</i>	I	Valid	N.E.	<i>r64</i> AND <i>r/m64</i> .

NOTES:

*In 64-bit mode, *r/m8* can not be encoded to access the following byte registers if a REX prefix is used: AH, BH, CH, DH.

AND—Logical AND

Opcode	Instruction	Op/ En	64-bit Mode	Compat/ Leg Mode	Description
24 <i>ib</i>	AND AL, <i>imm8</i>	RM	Valid	Valid	AL AND <i>imm8</i> .
25 <i>iw</i>	AND AX, <i>imm16</i>	RM	Valid	Valid	AX AND <i>imm16</i> .
25 <i>id</i>	AND EAX, <i>imm32</i>	RM	Valid	Valid	EAX AND <i>imm32</i> .
REX.W + 25 <i>id</i>	AND RAX, <i>imm32</i>	RM	Valid	N.E.	RAX AND <i>imm32</i> sign-extended to 64-bits.

- Opcode Column
- Represents the literal byte value(s) which correspond to the given instruction
- In this case, if you were to see a 0x24 followed by a byte or 0xAB followed by 4 bytes, you would know they were specific forms of the AND instruction.
 - Subject to correct interpretation under x86's multi-byte opcodes as discussed later.

AND—Logical AND

Opcode	Instruction	Op/ En	64-bit Mode	Compat/ Leg Mode	Description
24 <i>ib</i>	AND AL, <i>imm8</i>	RM	Valid	Valid	AL AND <i>imm8</i> .
25 <i>iw</i>	AND AX, <i>imm16</i>	RM	Valid	Valid	AX AND <i>imm16</i> .
25 <i>id</i>	AND EAX, <i>imm32</i>	RM	Valid	Valid	EAX AND <i>imm32</i> .
REX.W + 25 <i>id</i>	AND RAX, <i>imm32</i>	RM	Valid	N.E.	RAX AND <i>imm32</i> sign-extended to 64-bits.

- If it was 0x25, how would you know whether it should be followed by 2 bytes (*imm16*) or 4 bytes (*imm32*)? Because the same single opcode byte is used for both, the length of the operand depends on if the processor is in 16-bit, 32-bit, or 64-bit mode. Each mode has a default operand size (i.e. the size of the value).
- For 64-bit mode, the default operand size is 32-bits for most instructions and the default address size is 64-bits
- This means the default interpretation will usually be the ones with the *r/m32*, *r32*, *imm32*, or in this case a specific register like EAX

AND—Logical AND

Opcode	Instruction	Op/ En	64-bit Mode	Compat/ Leg Mode	Description
24 <i>ib</i>	AND AL, <i>imm8</i>	RM	Valid	Valid	AL AND <i>imm8</i> .
25 <i>iw</i>	AND AX, <i>imm16</i>	RM	Valid	Valid	AX AND <i>imm16</i> .
25 <i>id</i>	AND EAX, <i>imm32</i>	RM	Valid	Valid	EAX AND <i>imm32</i> .
REX.W + 25 <i>id</i>	AND RAX, <i>imm32</i>	RM	Valid	N.E.	RAX AND <i>imm32</i> sign-extended to 64-bits.

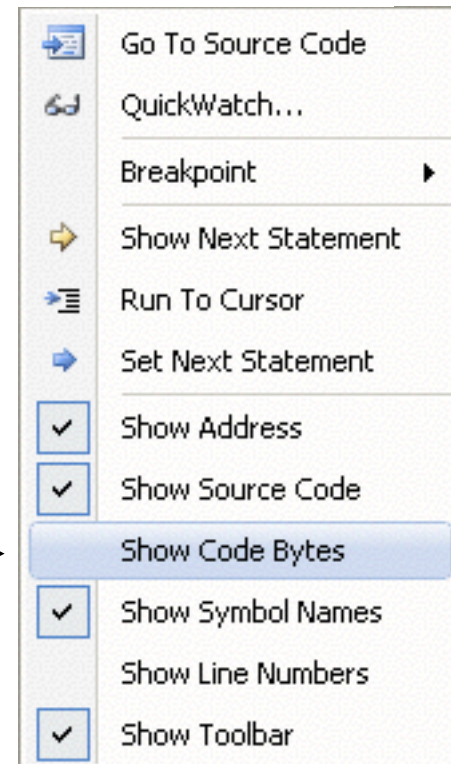
- In some cases the operand or address size can be overridden with special prefix bytes that come before the regular instruction opcode
- There are REX prefixes, address size prefixes, and operand size prefixes
- Will not go into detail for all of them, but the REX.W byte shown in this example (0x48) will cause the instruction to use 64-bit operands if in 64-bit mode (rather than 32-bit operands)
- Therefore, to encode this instruction to use 64-bit operands (RAX in this case), the code would have byte sequence 0x48 0x25 ...

AND—Logical AND

Opcode	Instruction	Op/En	64-bit Mode	Compat/Leg Mode	Description
24 <i>ib</i>	AND AL, <i>imm8</i>	RM	Valid	Valid	AL AND <i>imm8</i> .
25 <i>iw</i>	AND AX, <i>imm16</i>	RM	Valid	Valid	AX AND <i>imm16</i> .
25 <i>id</i>	AND EAX, <i>imm32</i>	RM	Valid	Valid	EAX AND <i>imm32</i> .
REX.W + 25 <i>id</i>	AND RAX, <i>imm32</i>	RM	Valid	N.E.	RAX AND <i>imm32</i> sign-extended to 64-bits.

- How to see the opcodes in VisualStudio:
- Seeing the exact opcode will help confirm the exact version of an Instruction

(to show bytes in gdb, use:
disassemble /r optionally passing
an address to disassemble at)



AND—Logical AND

Opcode	Instruction	Op/ En	64-bit Mode	Compat/ Leg Mode	Description
24 <i>ib</i>	AND AL, <i>imm8</i>	RM	Valid	Valid	AL AND <i>imm8</i> .
25 <i>iw</i>	AND AX, <i>imm16</i>	RM	Valid	Valid	AX AND <i>imm16</i> .
25 <i>id</i>	AND EAX, <i>imm32</i>	RM	Valid	Valid	EAX AND <i>imm32</i> .
REX.W + 25 <i>id</i>	AND RAX, <i>imm32</i>	RM	Valid	N.E.	RAX AND <i>imm32</i> sign-extended to 64-bits.

- Instruction Column
- The human-readable mnemonic which is used to represent the instruction.
- This will frequently contain special encodings such as the “r/mX format” which I’ve previously discussed

AND—Logical AND

Opcode	Instruction	Op/En	64-bit Mode	Compat/Leg Mode	Description
24 <i>ib</i>	AND AL, <i>imm8</i>	RM	Valid	Valid	AL AND <i>imm8</i> .
25 <i>iw</i>	AND AX, <i>imm16</i>	RM	Valid	Valid	AX AND <i>imm16</i> .
25 <i>id</i>	AND EAX, <i>imm32</i>	RM	Valid	Valid	EAX AND <i>imm32</i> .
REX.W + 25 <i>id</i>	AND RAX, <i>imm32</i>	RM	Valid	N.E.	RAX AND <i>imm32</i> sign-extended to 64-bits.

Should all be I, fixed in latest

- Operand Encoding Column
- This column was added in more recent manuals. I would find it more useful if there weren't so many errors :-/

Instruction Operand Encoding

Op/En	Operand 1	Operand 2	Operand 3	Operand 4
RM	ModRM:reg (r, w)	ModRM:r/m (r)	NA	NA
MR	ModRM:r/m (r, w)	ModRM:reg (r)	NA	NA
MI	ModRM:r/m (r, w)	<i>imm8</i>	NA	NA
I	AL/AX/EAX/RAX	<i>imm8</i>	NA	NA

Should allow for *imm8/16/32*, not fixed in latest

AND—Logical AND

Opcode	Instruction	Op/ En	64-bit Mode	Compat/ Leg Mode	Description
24 <i>ib</i>	AND AL, <i>imm8</i>	RM	Valid	Valid	AL AND <i>imm8</i> .
25 <i>iw</i>	AND AX, <i>imm16</i>	RM	Valid	Valid	AX AND <i>imm16</i> .
25 <i>id</i>	AND EAX, <i>imm32</i>	RM	Valid	Valid	EAX AND <i>imm32</i> .
REX.W + 25 <i>id</i>	AND RAX, <i>imm32</i>	RM	Valid	N.E.	RAX AND <i>imm32</i> sign-extended to 64-bits.

- 64bit Column
- Whether or not the opcode is valid in 64 bit mode.

AND—Logical AND

Opcode	Instruction	Op/ En	64-bit Mode	Compat/ Leg Mode	Description
24 <i>ib</i>	AND AL, <i>imm8</i>	RM	Valid	Valid	AL AND <i>imm8</i> .
25 <i>iw</i>	AND AX, <i>imm16</i>	RM	Valid	Valid	AX AND <i>imm16</i> .
25 <i>id</i>	AND EAX, <i>imm32</i>	RM	Valid	Valid	EAX AND <i>imm32</i> .
REX.W + 25 <i>id</i>	AND RAX, <i>imm32</i>	RM	Valid	N.E.	RAX AND <i>imm32</i> sign-extended to 64-bits.

- Compatibility/Legacy Mode Column
- Whether or not the opcode is valid in 32/16 bit code.
 - The N.E. Indicates an an instruction encoding which is only encodable in 64-bit mode

AND—Logical AND

Opcode	Instruction	Op/ En	64-bit Mode	Compat/ Leg Mode	Description
24 <i>ib</i>	AND AL, <i>imm8</i>	RM	Valid	Valid	AL AND <i>imm8</i> .
25 <i>iw</i>	AND AX, <i>imm16</i>	RM	Valid	Valid	AX AND <i>imm16</i> .
25 <i>id</i>	AND EAX, <i>imm32</i>	RM	Valid	Valid	EAX AND <i>imm32</i> .
REX.W + 25 <i>id</i>	AND RAX, <i>imm32</i>	RM	Valid	N.E.	RAX AND <i>imm32</i> sign-extended to 64-bits.

- Description Column
- Simple description of the action performed by the instruction
- Typically this just conveys the flavor of the instruction, but the majority of the details are in the main description text

80 /4 ib	AND <i>r/m8, imm8</i>	Valid	Valid	<i>r/m8 AND imm8.</i>
REX + 80 /4 ib	AND <i>r/m8[*], imm8</i>	Valid	N.E.	<i>r/m64 AND imm8 (sign-extended).</i>
81 /4 iw	AND <i>r/m16, imm16</i>	Valid	Valid	<i>r/m16 AND imm16.</i>
81 /4 id	AND <i>r/m32, imm32</i>	Valid	Valid	<i>r/m32 AND imm32.</i>

- Looking at some other forms, we now see those “r/mX” things I told you about
- We know that for instance it can start with an 0x80, and end with a byte, but what’s that /4?
- Unfortunately the explanation goes into too much detail for this class. Generally the only people who need to know it are people who want to write disassemblers. But I still put it in the Intermediate x86 class :)
- The main thing you need to know is that any time you see a r/mX, it can be either a register or memory value.

AND Details

- **Description**

- “Performs a bitwise AND operation on the destination (first) and source (second) operands and stores the result in the destination operand location. The source operand can be an immediate, a register, or a memory location; the destination operand can be a register or a memory location. (However, two memory operands cannot be used in one instruction.) Each bit of the result is set to 1 if both corresponding bits of the first and second operands are 1; otherwise, it is set to 0.

This instruction can be used with a LOCK prefix to allow the it to be executed atomically.”

- **Flags effected**

- “The OF and CF flags are cleared; the SF, ZF, and PF flags are set according to the result. The state of the AF flag is undefined.”

Jcc—Jump if Condition Is Met

Opcode	Instruction	Op/ En	64-Bit Mode	Compat/ Leg Mode	Description
77 <i>cb</i>	<i>JA rel8</i>	D	Valid	Valid	Jump short if above (CF=0 and ZF=0).
73 <i>cb</i>	<i>JAe rel8</i>	D	Valid	Valid	Jump short if above or equal (CF=0).
72 <i>cb</i>	<i>JB rel8</i>	D	Valid	Valid	Jump short if below (CF=1).
76 <i>cb</i>	<i>JBe rel8</i>	D	Valid	Valid	Jump short if below or equal (CF=1 or ZF=1).
72 <i>cb</i>	<i>JC rel8</i>	D	Valid	Valid	Jump short if carry (CF=1).
E3 <i>cb</i>	<i>JCXZ rel8</i>	D	N.E.	Valid	Jump short if CX register is 0.
E3 <i>cb</i>	<i>JECXZ rel8</i>	D	Valid	Valid	Jump short if ECX register is 0.
E3 <i>cb</i>	<i>JRCXZ rel8</i>	D	Valid	N.E.	Jump short if RCX register is 0.
74 <i>cb</i>	<i>JE rel8</i>	D	Valid	Valid	Jump short if equal (ZF=1).
7F <i>cb</i>	<i>JG rel8</i>	D	Valid	Valid	Jump short if greater (ZF=0 and SF=OF).
7D <i>cb</i>	<i>JGE rel8</i>	D	Valid	Valid	Jump short if greater or equal (SF=OF).
7C <i>cb</i>	<i>JL rel8</i>	D	Valid	Valid	Jump short if less (SF≠ OF).
7E <i>cb</i>	<i>JLE rel8</i>	D	Valid	Valid	Jump short if less or equal (ZF=1 or SF≠ OF).
76 <i>cb</i>	<i>JNA rel8</i>	D	Valid	Valid	Jump short if not above (CF=1 or ZF=1).
72 <i>cb</i>	<i>JNAe rel8</i>	D	Valid	Valid	Jump short if not above or equal (CF=1).
73 <i>cb</i>	<i>JNB rel8</i>	D	Valid	Valid	Jump short if not below (CF=0).
77 <i>cb</i>	<i>JNBe rel8</i>	D	Valid	Valid	Jump short if not below or equal (CF=0 and ZF=0).
73 <i>cb</i>	<i>JNC rel8</i>	D	Valid	Valid	Jump short if not carry (CF=0).
75 <i>cb</i>	<i>JNE rel8</i>	D	Valid	Valid	Jump short if not equal (ZF=0).
7E <i>cb</i>	<i>JNG rel8</i>	D	Valid	Valid	Jump short if not greater (ZF=1 or SF≠ OF).

Jcc Revisited

- If you look closely, you will see that there are multiple mnemonics for the same opcodes
- 0x77 = JA - Jump Above
- 0x77 = JNBE - Jump Not Below or Equal
- 0x74 = JE / JZ - Jump Equal / Zero
- Which mnemonic is displayed is disassembler-dependent

IMUL—Signed Multiply

Opcode	Instruction	Op/En	64-Bit Mode	Compat/Leg Mode	Description
F6 /5	IMUL <i>r/m8</i> *	M	Valid	Valid	AX ← AL * <i>r/m</i> byte.
F7 /5	IMUL <i>r/m16</i>	M	Valid	Valid	DX:AX ← AX * <i>r/m</i> word.
F7 /5	IMUL <i>r/m32</i>	M	Valid	Valid	EDX:EAX ← EAX * <i>r/m32</i> .
REX.W + F7 /5	IMUL <i>r/m64</i>	M	Valid	N.E.	RDX:RAX ← RAX * <i>r/m64</i> .
0F AF /r	IMUL <i>r16, r/m16</i>	RM	Valid	Valid	word register ← word register * <i>r/m16</i> .
0F AF /r	IMUL <i>r32, r/m32</i>	RM	Valid	Valid	doubleword register ← doubleword register * <i>r/m32</i> .
REX.W + 0F AF /r	IMUL <i>r64, r/m64</i>	RM	Valid	N.E.	Quadword register ← Quadword register * <i>r/m64</i> .
6B /r ib	IMUL <i>r16, r/m16, imm8</i>	RMI	Valid	Valid	word register ← <i>r/m16</i> * sign-extended immediate byte.
6B /r ib	IMUL <i>r32, r/m32, imm8</i>	RMI	Valid	Valid	doubleword register ← <i>r/m32</i> * sign-extended immediate byte.
REX.W + 6B /r ib	IMUL <i>r64, r/m64, imm8</i>	RMI	Valid	N.E.	Quadword register ← <i>r/m64</i> * sign-extended immediate byte.
69 /r iw	IMUL <i>r16, r/m16, imm16</i>	RMI	Valid	Valid	word register ← <i>r/m16</i> * immediate word.
69 /r id	IMUL <i>r32, r/m32, imm32</i>	RMI	Valid	Valid	doubleword register ← <i>r/m32</i> * immediate doubleword.
REX.W + 69 /r id	IMUL <i>r64, r/m64, imm32</i>	RMI	Valid	N.E.	Quadword register ← <i>r/m64</i> * immediate doubleword.

NOTES:

* In 64-bit mode, *r/m8* can not be encoded to access the following byte registers if a REX prefix is used: AH, BH, CH, DH.

Instruction Operand Encoding

Op/En	Operand 1	Operand 2	Operand 3	Operand 4
M	ModRM:r/m (r, w)	NA	NA	NA
RM	ModRM:reg (r, w)	ModRM:r/m (r)	NA	NA
RMI	ModRM:reg (r, w)	ModRM:r/m (r)	imm8/16/32	NA

IMUL Revisited

- Scavenger hunt: for “extra credit” (i.e. getting credited in the slides ;)) find me another “basic” instruction, that’s not part of a special add-on instruction set (like VMX, SMX, MMX, SSE*, AES, AVX, etc) and isn’t a floating point instruction, which uses ≥ 3 operands
- hint: if you see a “CPUID feature flag” column, it means it’s a special instruction set

Instruction Operand Encoding

Op/En	Operand 1	Operand 2	Operand 3	Operand 4
M	ModRM:r/m (r, w)	NA	NA	NA
RM	ModRM:reg (r, w)	ModRM:r/m (r)	NA	NA
RMI	ModRM:reg (r, w)	ModRM:r/m (r)	imm8/16/32	NA