

Introduction to Intel x86-64 Assembly, Architecture, Applications, & Alliteration

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Digression – Why Two's Complement?

- Alternative methods of representing negative numbers (signed magnitude, or just ones complement), as well as their problems presented on page 166-167 of the 32 bit book.
 - Note to self: show on board quick
- The benefit of two's complement is due to having only one representation of zero, and being able to reuse the same hardware for addition/subtraction
- Dave Keppler suggested expanding on this

Why Two's Complement? 2

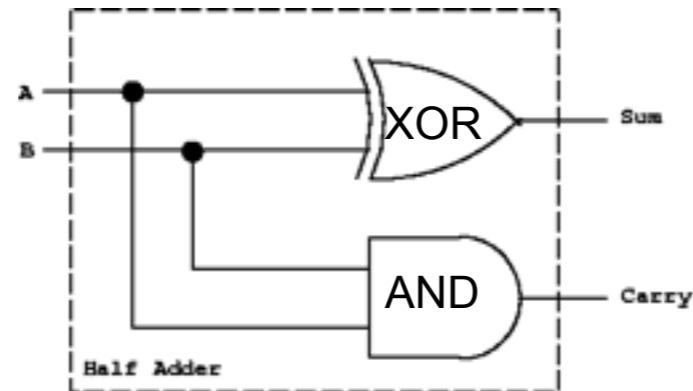
$$\begin{array}{r}
 \text{Carry} \\
 \swarrow \quad \searrow \\
 1 \qquad \qquad 1 \\
 \begin{array}{r}
 5d \\
 + 6d \\
 \hline
 11d
 \end{array}
 \qquad
 \begin{array}{r}
 1b \\
 + 1b \\
 \hline
 10b
 \end{array}
 \end{array}$$

Binary/Decimal Inputs		Decimal Result	Binary Result
A	B	D	$Y_1 Y_0$
0	0	0	0 0
0	1	1	0 1
1	0	1	0 1
1	1	2	1 0

Table taken from
http://thalia.spec.gmu.edu/~pparis/classes/notes_101/node110.html

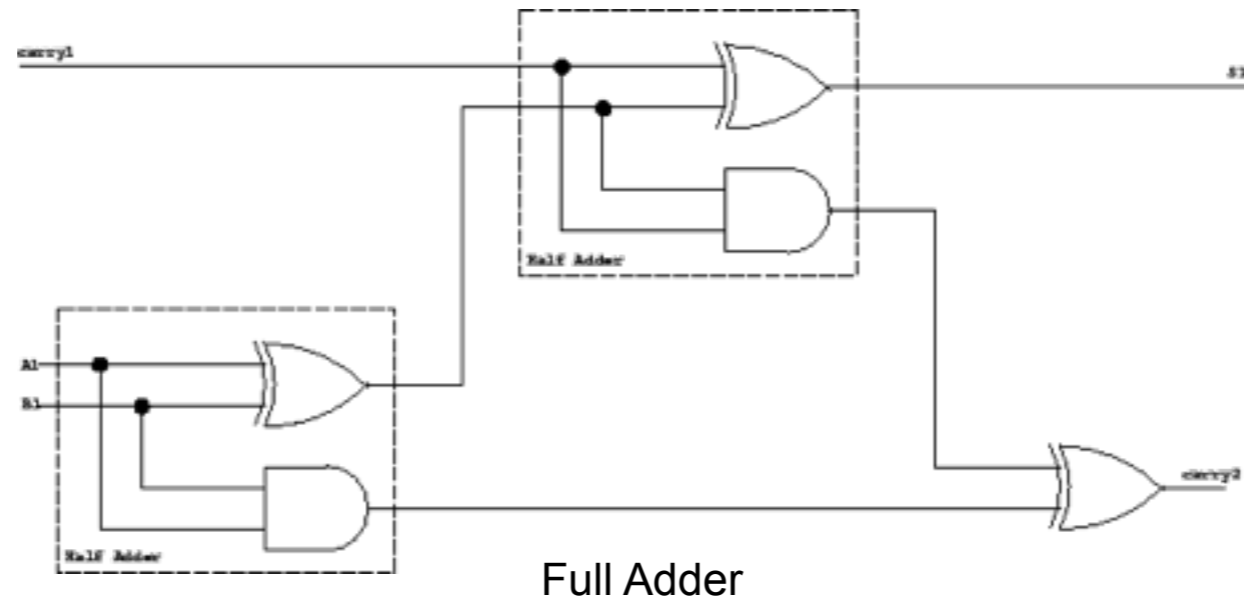
Why Two's Complement? 3

A half adder circuit suffices for one bit addition



Picture taken from
http://thalia.spec.gmu.edu/~pparis/classes/notes_101/node110.html

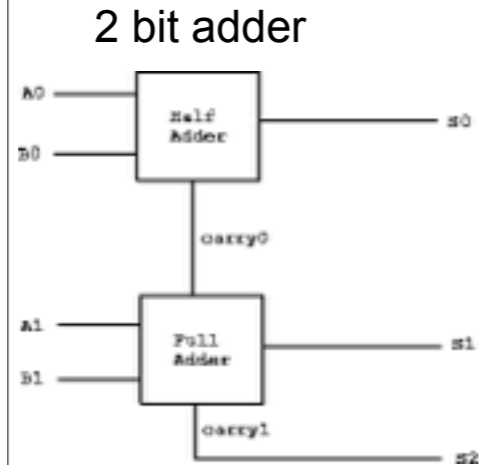
Why Two's Complement? 4



You can't just chain the one bit half adders together to get multi-bit adders. To see why, see the truth table at the link.

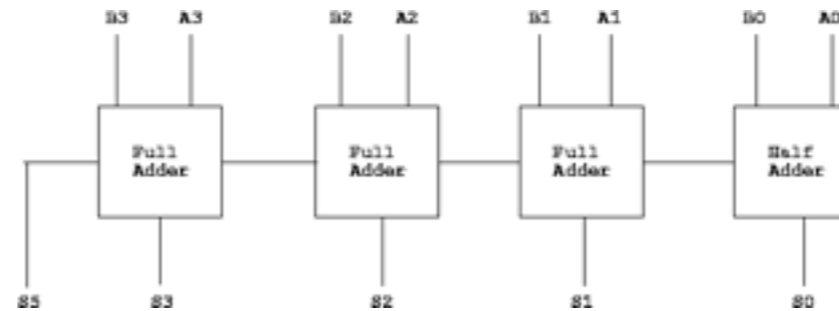
Picture taken from
http://thalia.spec.gmu.edu/~pparis/classes/notes_101/node111.html

Why Two's Complement? 5



Note: we start with a half adder because a full adder would need a carry input at the start. However, if we wanted to use this for subtraction we could use a full adder to start. More on this on next slide.

4 bit adder
(continue to make n bit adder)



Pictures taken from

http://thalia.spec.gmu.edu/~pparis/classes/notes_101/node112.html

http://thalia.spec.gmu.edu/~pparis/classes/notes_101/node113.html

Why Two's Complement? 6

- So you have these physical adder circuits in the Arithmetic Logic Unit (ALU), and you can feed both add and subtract to the same circuit. But for this to work, you need to start with a full adder, and then run one the one subtract operand bits through not gates, and then set carry to one on the first full adder.
- Kepler's example of $x-y == x+(-y)$
 - Cause it was right there in my email and I'm lazy ;)

00001010	00001010 (10d)	==	00001010 (10d)
+ 00000101	-00000101 (5d)		+11111011 (-5d)
-----	-----		-----
00001111	00000101		1 00000101